

### **Remarks**

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. Claims 1-3 have been cancelled. New claims 4-23 have been added. Therefore, claims 4-23 are presented for examination.

Replacement drawings are submitted herewith.

Claims 1-3 stand rejected under 35 U.S.C. §102(b) as being anticipated by Dye et al. (U.S. Patent No. 6,145,069). Applicants submit that the present claims are patentable over Dye.

Dye discloses a flash memory controller and/or embedded memory controller including MemoryF/X Technology that uses data compression and decompression for improved system cost and performance. The Compression Enhanced Flash Memory Controller (CEPMC) uses parallel lossless compression and decompression engines embedded into the flash memory controller unit for improved memory density and data bandwidth. In addition, a Compression Enhanced Memory Controller (CEMC) is included where the parallel compression and decompression engines are introduced into the memory controller of the microprocessor unit. The CEMC improves system wide memory density and data bandwidth. See Dye at Abstract.

Claim 4 of the present application recites a memory controller having a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format. Applicants submit that Dye fails to disclose the implementation of a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format. Thus claim 4 is patentable over Dye.

Claims 5-11 depend from claim 4 and include additional features. Thus, claims 5-11 are also patentable over Dye.

Claim 12 recites updating a compression map within a memory controller to indicate the one or more cache lines corresponding to a block of data in a system memory are in a compressed format. For the reasons described above with respect to claim 4, claim 12 is also patentable over Dye. Because claims 13-16 depend from claim 12 and include additional features, claims 13-16 are also patentable over Dye.

Claim 17 recites a memory controller having a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format. Therefore, for the reasons described above with respect to claim 4, claim 17 is also patentable over Dye. Since claims 18-23 depend from claim 17 and include additional features, claims 18-23 are also patentable over Dye.

Claim 3 stands rejected under 35 U.S.C. §102(e) as being anticipated by Naffziger et al. (U.S. Pub. No. 2003/0135694). Applicants submit that the present claims are patentable over Naffziger.

Naffziger discloses a compression engine for a cache memory subsystem that has a pointer into cache tag memory and cache data memory and an interface coupled to the pointer and capable of being coupled to cache tag memory, and cache data memory. The interface reads tag information and uncompressed data from the cache and writes modified tag information and compressed data to the cache. The compression engine also has compression logic for generating compressed data and generating compression successful information, and tag line update circuitry for generating modified tag information according

to the compression successful information and the tag information. See Naffziger at Abstract.

Nevertheless, nowhere in Naffziger is there disclosed a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format. Accordingly, the present claims are patentable over Naffziger.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.


The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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